REMARKS

The Examiner rejected claims 17-19, 22, 24-26, 32 and 33 under 35 U.S.C. § 102(b) as allegedly being anticipated by Wong (U.S. 6,340,556).

The Examiner rejected claims 1-3, 5, 8 and 28 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838).

The Examiner rejected claim 6 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838) as applied to claim 1 above, and further in view of Cowan (U.S. 6,605,951).

The Examiner rejected claims 10-12, 15 and 31 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Wolf *et al.* (*Silicon Processing for the VLSI Era*, Vol. 1, 2000).

The Examiner rejected claims 7 and 9 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838), as applied to claim 1 above, and further in view of Ghandhi (*VLSI Fabrication Principles - Silicon and Gallium Arsenide, Second Edition*, 1994).

The Examiner rejected claims 14 and 16 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Wolf *et al.* (*Silicon Processing for the VLSI Era*, Vol. 1, 2000) as applied to claims 10 and 15 above, and further in view of Ghandi (*VLSI Fabrication Principles - Silicon and Gallium Arsenide*. Second Edition, 1994).

The Examiner rejected claims 21 and 23 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Ghandi (*VLSI Fabrication Principles - Silicon and Gallium Arsenide*, Second Edition, 1994).

The Examiner rejected claim 4 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838) as applied to claim 1 above, and further in view of Okoroanyanwy (U.S. 2002/0160628).

The Examiner rejected claim 13 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Wolf *et al.* (*Silicon Processing for the VLSI Era*, Vol. 1, 2000) as applied to claim 10 above, and further in view of Okoroanyanwy (U.S. 2002/0160628).

The Examiner rejected claims 20 and 27 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Okoroanyanwy (U.S. 2002/0160628).

The Examiner rejected claim 29 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838) and Cowan (U.S. 6,605,951) as applied to claim 6 above, and in further view of Lowell et. Al. (U.S. 5,963,783).

The Examiner rejected claim 30 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838) and Cowan (U.S. 6,605,951) as applied to claim 6 above, and in further view of Bode et. Al. (U.S. 6,937,914).

Applicants respectfully traverse the § 102 and § 103 rejections with the following arguments.

35 U.S.C. § 102(b)

Claims 17-19, 22, 24-26, 32 and 33 are rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Wong (U.S. 6,340,556).

Applicants respectfully contend that Wong does not anticipate claims 17 and 24 as amended, because Wong does not teach each and every feature of claims 17 and 24.

For example, Wong does not teach the feature of "forming a plurality of features in the photo resist layer; measuring a plurality of critical dimensions...to determine at least one critical dimension error...correcting the at least one critical dimension error by **selectively** exposing **only the at least one feature** comprising the critical dimension error to an electron beam comprising said determined dose of electron beam exposure that corrects the critical dimension error of the at least one feature" (emphasis added).

The Examiner alleges that " Wong teaches a method, comprising...correcting the at least one critical dimension error by selectively exposing only the at least one feature comprising the critical dimension error to an electron beam comprising said determined dose of electron beam exposure that corrects the critical dimension error of the at least one feature (Wong teaches exposing the remaining photo resist layer, which is made up of only the features requiring correction, to an electron beam in order to reduce the linewidth of the features-column 8, lines 7-67)".

In response, Applicants respectfully contend that Wong does not teach that **only** at least one feature (i.e., formed in a photo resist layer) comprising a critical dimension error is **selectively exposed** to an electron beam that corrects the critical dimension error as taught by Applicant's claims 17 and 24. In contrast, Wong teaches in col. 8, lines 18-22 that " The electron

beam irradiating is conducted with a uniform, large-area, overall electron beam exposure source which **simultaneously** exposes substantially **all of the image areas** of the photosensitive composition **simultaneously**". Wong further teaches in Col. 8, lines 52-54 " the electron beam exposing step is conducted with a wide, large beam of electron beam radiation from a uniform large-area electron beam source which **simultaneously** covers the **entire substrate** " Therefore, Applicants contend that Wong teaches a process for exposing an **entire substrate** comprising a **plurality of photo resist lines** (i.e.,Wong teaches photo resist lines **and** the substrate are exposed simultaneously) to electron beam radiation. Applicants argue that Wong does not teach **selectively exposing only** a photo resist feature(s) and **not a substrate** to an electron beam as taught by Applicant's claims 17 and 24. In fact, Wong teaches a "large-area electron beam source which **simultaneously covers the entire substrate** "(i.e., the photosensitive composition **and** the substrate comprising the photosensitive composition).

The Examiner further alleges in response to Applicant's arguments filed on 6/26/2006 in response to the office action mailed on 3/30/06 that "Applicant primarily argues that Wong does not anticipate the claims as amended, specifically because Wong teaches exposing more than only the feature comprising the critical dimension error. However, this argument is not persuasive because although Wong exposes all of the features of a device, they all contain critical dimension errors, so Wong does teach selectively exposing only the features comprising a critical dimension error "

In response, Applicant's contend that Wong does not teach that **only** at least one feature (and not the substrate) comprising a critical dimension error is **selectively exposed** to an electron beam as taught by as taught by Applicant's claims 17 and 24. In contrast, Wong teaches

a "large-area electron beam source which **simultaneously covers the entire substrate** "(i.e., the photosensitive composition **and** the substrate comprising the photosensitive composition). Therefore, Applicants contend that Wong does not selectively expose only a feature (and not the substrate) comprising a critical dimension error.

Based on the preceding arguments, Applicants respectfully maintain that Wong does not anticipate claims 17 and 24 and that claims 17 and 24 are in condition for allowance. Since claims 18, 19, 22, and 32 depend from claim 17 and claims 24-26 and 33 depend from claim 24, Applicants contend that claims 18, 19, 22, 24-26, 31 and 32 are likewise in condition for allowance.

35 U.S.C. § 103(a)

Claims 1-3, 5, 8 and 28

Claims 1-3, 5, 8 and 28 rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838).

Applicants respectfully contend that claim 1 is not unpatentable over Wong in view of Marella, because Wong and Marella do not teach or suggest each and every feature of claim 1.

For example, Wong and Marella do not teach or suggest the feature of "forming a plurality of features in the photo resist layer; measuring a plurality of critical dimensions...to determine at least one critical dimension error...correcting the at least one critical dimension error by **selectively** exposing **only the at least one feature** comprising the critical dimension error to an electron beam comprising said determined dose of electron beam exposure that corrects the critical dimension error of the at least one feature" (emphasis added).

The Examiner alleges that "Wong teaches a method, comprising...correcting the at least one critical dimension error by selectively exposing only the at least one feature comprising the critical dimension error to an electron beam comprising said determined dose of electron beam exposure that corrects the critical dimension error of the at least one feature (Wong teaches exposing the remaining photo resist layer, which is made up of only the features requiring correction, to an electron beam in order to reduce the linewidth of the features-column 8, lines 7-67)".

In response, Applicants respectfully contend that Wong and Marella do not individually or in combination teach or suggest that **only** at least one feature (i.e., formed in a photo resist layer) comprising a critical dimension error is **selectively exposed** to an electron beam that

corrects the critical dimension error as taught by Applicant's claim 1. In contrast, Wong teaches in col. 8, lines 18-22 that " The electron beam irradiating is conducted with a uniform, large-area, overall electron beam exposure source which **simultaneously** exposes substantially **all of the image areas** of the photosensitive composition **simultaneously**". Wong further teaches in Col. 8, lines 52-54 " the electron beam exposing step is conducted with a wide, large beam of electron beam radiation from a uniform large-area electron beam source which **simultaneously** covers the **entire substrate** " Therefore, Applicants contend that Wong teaches a process for exposing an **entire substrate** comprising a **plurality of photo resist lines** (i.e.,Wong teaches photo resist lines **and** the substrate are exposed simultaneously) to electron beam radiation. Applicants argue that Wong does not teach **selectively exposing only** a photo resist feature(s) and **not a substrate** to an electron beam as taught by Applicant's claim 1. In fact, Wong teaches a "large-area electron beam source which **simultaneously covers the entire substrate** "(i.e., the photosensitive composition **and** the substrate comprising the photosensitive composition).
The Examiner further alleges in response to Applicant's arguments filed on 6/26/2006 in response to the office action mailed on 3/30/06 that "Applicant primarily argues that Wong does not anticipate the claims as amended, specifically because Wong teaches exposing more than only the feature comprising the critical dimension error. However, this argument is not persuasive because although Wong exposes all of the features of a device, they all contain critical dimension errors, so Wong does teach selectively exposing only the features comprising a critical dimension error "

In response, Applicant's contend that Wong does not teach that **only** at least one feature (and not the substrate) comprising a critical dimension error is **selectively exposed** to an electron beam as taught by as taught by Applicant's claim 1. In contrast, Wong teaches a "large-area electron beam source which **simultaneously covers the entire substrate** "(i.e., the photosensitive composition **and** the substrate comprising the photosensitive composition).

Therefore, Applicants contend that Wong does not selectively expose only a feature (and not the substrate) comprising a critical dimension error.

Based on the preceding arguments, Applicants respectfully maintain that claim 1 is not unpatentable over Wong in view of Marella, and that claim 1 is in condition for allowance. Since claims 2, 3, 5, 8 and 28 depend from claim 1, Applicants contend that claims 2, 3, 5, 8 and 28 are likewise in condition for allowance.

Claim 6

Claim 6 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838) as applied to claim 1 above, and further in view of Cowan (U.S. 6,605,951).

In response, Applicants contend that since claim 6 depends from claim 1 which Applicants have argued *supra* to not be unpatentable over Wong in view of Marella under 35 U.S.C. §103(a), Applicants maintain that claim 6 is likewise not unpatentable Wong in view of Marella and further in view of Cowan under 35 U.S.C. §103(a).

Claims 10-12, 15, and 31

Claims 10-12, 15, and 31 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Wolf *et al.* (*Silicon Processing for the VLSI Era*, Vol. 1, 2000).

Applicants respectfully contend that claim 10 as amended is not unpatentable over Wong in view of Wolf, because Wong and Wolf do not teach or suggest each and every feature of claim 10.

For example, Wong and Wolf do not teach or suggest the feature of "forming a plurality of features in the photo resist layer; measuring a plurality of critical dimensions...to determine at least one critical dimension error...correcting the at least one critical dimension error by **selectively** exposing **only the at least one feature** comprising the critical dimension error to an electron beam comprising said determined dose of electron beam exposure that corrects the critical dimension error of the at least one feature" (emphasis added).

The Examiner alleges that "Wong teaches a method, comprising...correcting the at least one critical dimension error by selectively exposing only the at least one feature comprising the critical dimension error to an electron beam comprising said determined dose of electron beam exposure that corrects the critical dimension error of the at least one feature (Wong teaches exposing the remaining photo resist layer, which is made up of only the features requiring correction, to an electron beam in order to reduce the linewidth of the features-column 8, lines 7-67)".

In response, Applicants respectfully contend that Wong and Wolf do not individually or in combination teach or suggest that **only** at least one feature (i.e., formed in a photo resist layer) comprising a critical dimension error is **selectively exposed** to an electron beam that corrects the critical dimension error as taught by Applicant's claim 10. In contrast, Wong teaches in col. 8, lines 18-22 that " The electron beam irradiating is conducted with a uniform, large-area, overall electron beam exposure source which **simultaneously** exposes substantially **all of the image areas** of the photosensitive composition **simultaneously**". Wong further teaches in Col. 8, lines 52-54 " the electron beam exposing step is conducted with a wide, large beam of electron beam radiation from a uniform large-area electron beam source which **simultaneously** covers the

entire substrate " Therefore, Applicants contend that Wong teaches a process for exposing an **entire substrate** comprising a **plurality of photo resist lines** (i.e.,Wong teaches photo resist lines **and** the substrate are exposed simultaneously) to electron beam radiation. Applicants argue that Wong does not teach **selectively exposing only** a photo resist feature(s) and **not a substrate** to an electron beam as taught by Applicant's claim 10. In fact, Wong teaches a "large-area electron beam source which **simultaneously covers the entire substrate** "(i.e., the photosensitive composition **and** the substrate comprising the photosensitive composition).

The Examiner further alleges in response to Applicant's arguments filed on 6/26/2006 in response to the office action mailed on 3/30/06 that "Applicant primarily argues that Wong does not anticipate the claims as amended, specifically because Wong teaches exposing more than only the feature comprising the critical dimension error. However, this argument is not persuasive because although Wong exposes all of the features of a device, they all contain critical dimension errors, so Wong does teach selectively exposing only the features comprising a critical dimension error "

In response, Applicant's contend that Wong does not teach that **only** at least one feature (and not the substrate) comprising a critical dimension error is **selectively exposed** to an electron beam as taught by as taught by Applicant's claim 10. In contrast, Wong teaches a "large-area electron beam source which **simultaneously covers the entire substrate** "(i.e., the photosensitive composition **and** the substrate comprising the photosensitive composition). Therefore, Applicants contend that Wong does not selectively expose only a feature (and not the substrate) comprising a critical dimension error.

Based on the preceding arguments, Applicants respectfully maintain that claim 10 is not unpatentable over Wong in view of Wolf, and that claim 10 is in condition for allowance. Since claims 10-12, 15, and 31 depend from claim 10, Applicants contend that claims 10-12, 15, and 31 are likewise in condition for allowance.

Claims 7 and 9

Claims 7 and 9 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838), as applied to claim 1 above, and further in view of Ghandhi (*VLSI Fabrication Principles - Silicon and Gallium Arsenide, Second Edition*, 1994).

In response, Applicants contend that since claims 7 and 9 depends from claim 1 which Applicants have argued *supra* to not be unpatentable over Wong in view of Marella under 35 U.S.C. §103(a), Applicants maintain that claims 7 and 9 are likewise not unpatentable Wong in view of Marella and further in view of Ghandhi under 35 U.S.C. §103(a).

Claims 14 and 16

Claims 14 and 16 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Wolf *et al.* (*Silicon Processing for the VLSI Era*, Vol. 1, 2000) as applied to claims 10 and 15 above, and further in view of Ghandi (*VLSI Fabrication Principles - Silicon and Gallium Arsenide*. Second Edition, 1994).

In response, Applicants contend that since claims 14 and 16 depend from claim 10 which Applicants have argued *supra* to not be unpatentable over Wong in view of Wolf under 35

U.S.C. § 103(a), Applicants maintain that claims 14 and 16 are likewise not unpatentable Wong in view of Marella and further in view of Ghandhi under 35 U.S.C. §103(a).

Claims 21 and 23

Claims 21 and 23 rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Ghandi (*VLSI Fabrication Principles - Silicon and Gallium Arsenide*, Second Edition, 1994).

In response, Applicants contend that since claims 21 and 23 depend from claim 17 which Applicants have argued *supra* to not be anticipated by Wong under 35 U.S.C. §102(b), Applicants maintain that claims 21 and 23 are likewise not unpatentable over Wong in view of Ghandi under 35 U.S.C. §103(a).

Claim 4

Claim 4 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838) as applied to claim 1 above, and further in view of Okoroanyanwy (U.S. 2002/0160628).

In response, Applicants contend that since claim 4 depends from claim 1 which Applicants have argued *supra* to not be unpatentable over Wong in view of Marella under 35 U.S.C. §103(a), Applicants maintain that claim 4 are likewise not unpatentable Wong in view of Marella and further in view of Okoroanyanwy under 35 U.S.C. §103(a).

Claim 13

Claims 13 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Wolf *et al.* (*Silicon Processing for the VLSI Era*, Vol. 1, 2000) as applied to claim 10 above, and further in view of Okoroanyanwy (U.S. 2002/0160628).

In response, Applicants contend that since claim 13 depends from claim 10 which Applicants have argued *supra* to not be unpatentable over Wong in view of Wolf under 35 U.S.C. § 103(a), Applicants maintain that claim 13 is likewise not unpatentable over Wong in view of Wolf and further in view of Okoroanyanwy under 35 U.S.C. §103(a).

Claims 20 and 27

Claims 20 and 27 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Okoroanyanwy (U.S. 2002/0160628).

In response, Applicants contend that since claim 20 depends from claim 17 and claim 27 depends from claim 24 which Applicants have argued *supra* to not be anticipated by Wong under 35 U.S.C. §102(b), Applicants maintain that claims 20 and 27 are likewise not unpatentable over Wong in view of Okoroanyanwy under 35 U.S.C. §103(a).

Claim 29

Claim 29 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838) and Cowan (U.S. 6,605,951) as applied to claim 6 above, and in further view of Lowell et. al. (U.S. 5,963,783).

In response, Applicants contend that since claim 29 depends from claim 1which Applicants have argued *supra* to not be anticipated by Wong under 35 U.S.C. §102(b),

Applicants maintain that claim 29 is likewise not unpatentable over Wong, Marella, Cowan, and Lowell under 35 U.S.C. §103(a).

Claim 30

Claim 30 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Wong (U.S. 6,340,556) in view of Marella (U.S. 2003/0139838) and Cowan (U.S. 6,605,951) as applied to claim 6 above, and in further view of Bode et. Al. (U.S. 6,937,914).

Applicants respectfully contend that claim 30 is not unpatentable over Wong in view of Marella and Cowan and in further view of Bode because Wong, Marella, Cowan, ,and Bode do not teach or suggest each and every feature of claim 30.

For example, Wong, Marella, Cowan, and Bode do not teach or suggest the feature of "wherein said analyzing further comprises **comparing** said plurality of operating conditions to a plurality of **actual operating characteristics of a second semiconductor device known to comprise no CD errors**" (emphasis added).

The Examiner alleges that "Bode et al. teaches analyzing devices for critical dimension errors by comparing operating conditions of a device against the operating characteristics of other devices, some known to comprise no CD errors (Fig. 2 shows a plot of operating characteristics as a function of CD error-0 is no error; column 5, lines 35-49)"

In response, Applicants respectfully contend that Bode does not teach or suggest an analysis process comprising comparing actual operating conditions of a first device to **actual operating characteristics of a second device known to comprise no CD errors**. In contrast, Bode teaches in col. 5, lines 35-49 " FIG. 2 is a graph 200 illustrating how a particular device

characteristic controlled by a process controller 80 based on a target value correlates to various manufacturing metrics...The values on the x-axis represent deviations from the target value 210 in units (e.g., each unit could represent 1 nanometer). For actual devices fabricated in the manufacturing system 10, the critical dimensions are measured and associated with manufacturing metrics determined for the completed devices." Therefore, Applicants contend that Bode teaches comparing target values to actual values. Applicants argue that Bode does not specify a **second device known to comprise no CD errors** as taught by Applicant's claim 30. Applicant' further contend that the Examiner has incorrectly concluded that the target value 210 of Bode represents the **second device known to comprise no CD errors** of Applicant's claim 30. In response, Applicants argue that Bode only teaches comparing target values to actual values and does not specify that the target values are derived from a **second device known to comprise no CD errors**. Based on the preceding arguments, Applicants respectfully maintain that claim 30 is not unpatentable over Wong, Marella, Cowan, and Bode and that claim 30 is in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Date: 9/15/06

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